

FPL 2019

High-performance Decoding of Variable-length Memory Data Packets for FPGA Stream Processing



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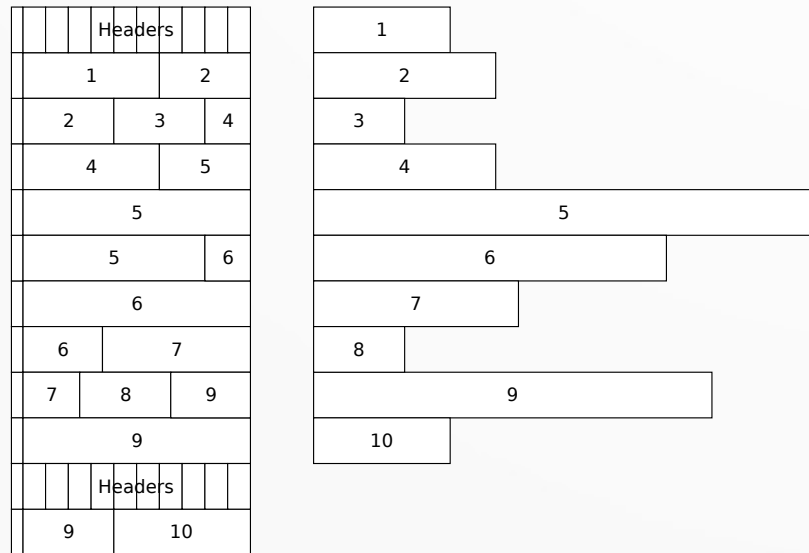
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Motivation

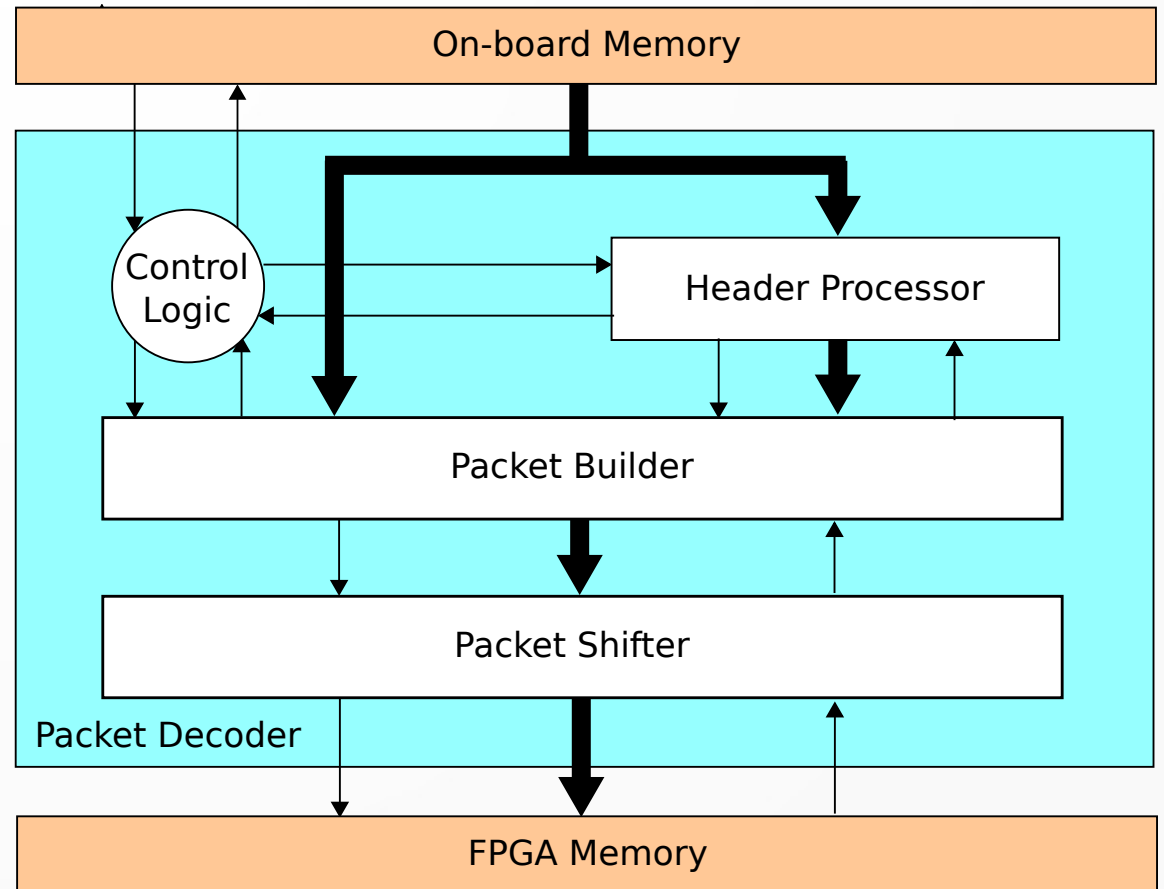
- Variable-length data is used to efficiently compress mesh-based datasets in scientific applications (e.g., CFD)
- Streaming variable-length data from memory to FPGA devices with a fixed-length encoding leads to wasting storage and bandwidth
- Each algorithm (e.g., 2D/3D, custom arithmetic formats) needs a different set of data packet lengths
 - Known at synthesis time

Our proposal: Architecture

- Parameterizable
- Fully pipelined
- Elastic interfaces (valid/ready)
- 1 packet/line per clock cycle



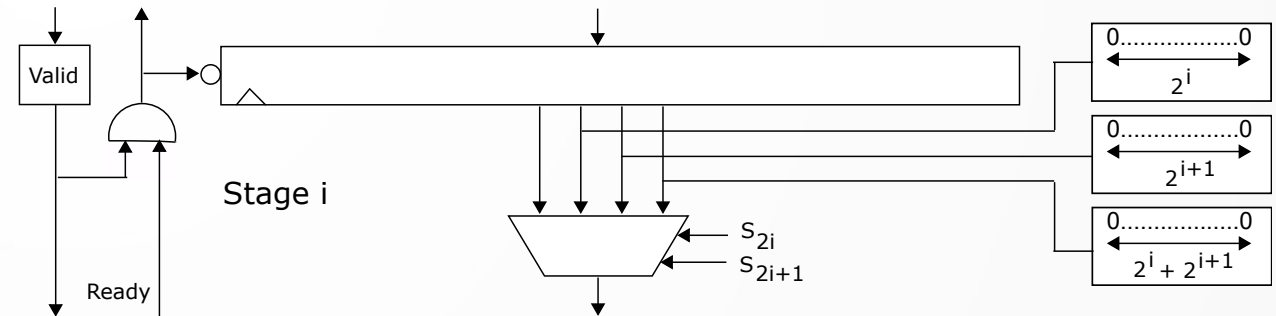
Example input and output



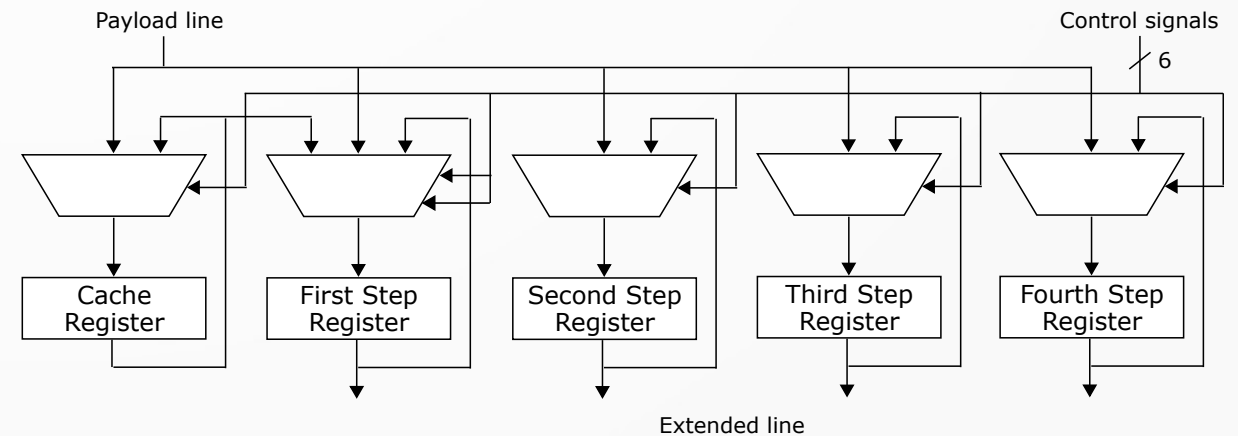
Overall architecture

Architecture (II)

- Packet Shifter:
 - Unfortunately, no barrel shifter in FPGAs
 - 4-1 (or 2-1) shifter stages
- Packet Builder:
 - Concatenate memory lines
- Header Decoder:
 - Computes shift and number of lines needed by each packet



Packet Shifter stage



Packet Builder

Results

- Synthesis results of example decoders

Decoder	A	B	C	D
Memory width (B)	128	128	200	256
Packet lengths	15	39	15	39
Max length (M)	120	252	368	497
ALMs	790	1491	2360	3121
Registers	1337	2095	3047	3918
Frequency (MHz)	438.02	488.52	494.07	457.46

Stratix V 5SGXMABN3F45C2

- Speedup over fixed-length encoding

Decoder	Hybrid speedup	Variable speedup
A	x1.069115	x1.523079
B	x1.356775	x2.157510
C	x1.358741	x1.932386
D	x1.491203	x2.350861

Thank you!