Limago: an FPGA-based Open-Source 100 GbE TCP/IP Stack

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Motivation

- Network is becoming a bottleneck in current datacenter applications.
- New approaches are being explored to maximize the network efficiency and to tailor its functionality to the actual needs.
- In-network data processing.
- Network-attached paradigm.
- Provide a platform for further research in programmable networks.
- Starting point 10 Gbit/s stack by Sidler et al. [1]

Challenges

- Datapath 8x, clock frequency 2x
- Scalability with increasing network bandwidth.
- Flexible and high-productivity methodology. Vivado-HLS
- Widen applicability.
- Long Fat Pipe Issue.
  \[RTT(s) \times LinkCapacity(b/s) > BufferSize(b)\]
- One’s complement checksum [2].
- CAM. New design based on cuckoo hashing (HLS).
- DRAM bandwidth.

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**Limago at a Glance**

- 4x128-bit LBUS @ 322 MHz
- 512-bit AXI4-S @ 322 MHz

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**Diagram:**

- Ultrascale+ Integrated 100 G Ethernet Subsystem
- LBUS-AXI4-S Adapter
- Inbound Packet Handler
- ARP
- Outbound Packet Handler
- ICMP
- TOE
- DMA Subsystem
- Application
- MIG
- External DDR4
- AXI4-S
- AXI4-Lite

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Experiments

Limago to Limago (running iperf2 one connection)

Measured Throughput Over Different Schemes

- Scheme 1 (Link Bounded)
- Scheme 2 (DRAM Bounded)
- Scheme 2(b) (Design Bounded)
Experiments

Server(s) to Limago (running iperf2)

Throughput for concurrent connections

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Resource consumption (TOE)

Linear Scaling

Number of Connections

512  1024  2048  4096  8192  16384

Number of BRAM for a given Window Scale and number of connections

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Conclusions

✓ Open-Source implementation.
✓ Support for multiple connections and Window Scale.
✓ Mostly written in C/C++ using Vivado-HLS.
✓ 7,456 lines of C/C++ and 1,482 lines of HDL.
✓ Future work includes support for packet reordering and selective acknowledgement (using HBM).

<table>
<thead>
<tr>
<th>VCU118</th>
<th>LUT</th>
<th>FF</th>
<th>BRAM</th>
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<tr>
<td>10 G</td>
<td>6.6 %</td>
<td>3.6 %</td>
<td>17.1 %</td>
</tr>
<tr>
<td>100 G</td>
<td>10.1 %</td>
<td>7.5 %</td>
<td>20.4 %</td>
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<tr>
<td>Difference</td>
<td>1.55x</td>
<td>2.1x</td>
<td>1.2x</td>
</tr>
</tbody>
</table>

Just 20 % more BRAM for 10x throughput
Visit our poster for further details

Check out our github!