



FPL 2019

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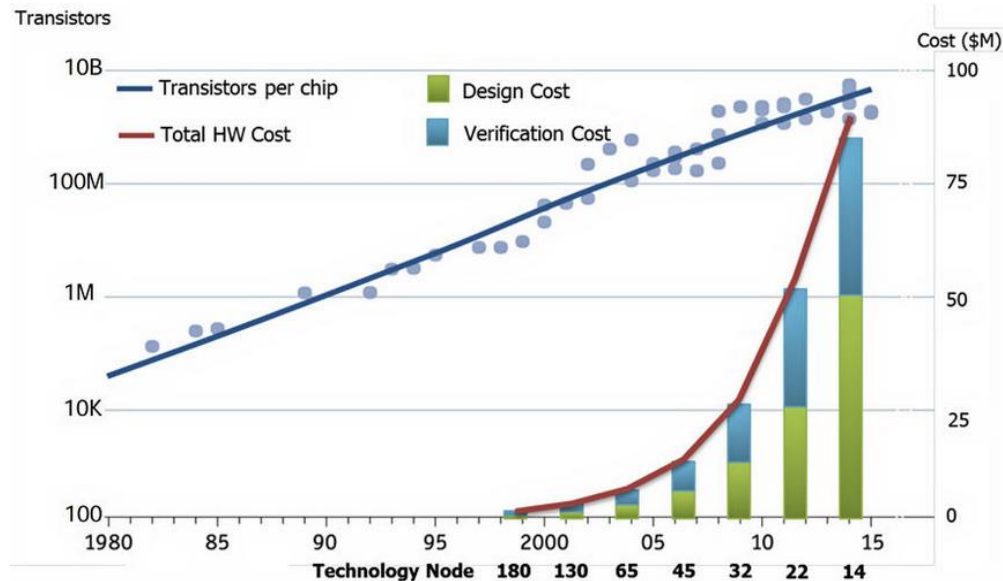
Analysis of Performance Variation in 16 nm FinFET FPGA Devices

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Ioannis Stratakos, Dimitrios Soudris**

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Introduction

- Further transistor scaling has become extremely challenging



Source: DARPA, <http://www.ispd.cc/slides/2018/k2.pdf>

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- Further transistor scaling has become extremely challenging
- Increased **process variability**
 - great **deviations in electrical properties** of transistors
 - switching activity, leakage current
- Global & pessimistic operation guard-bands are employed
 - **performance loss**, i.e., maximum frequency, power consumption

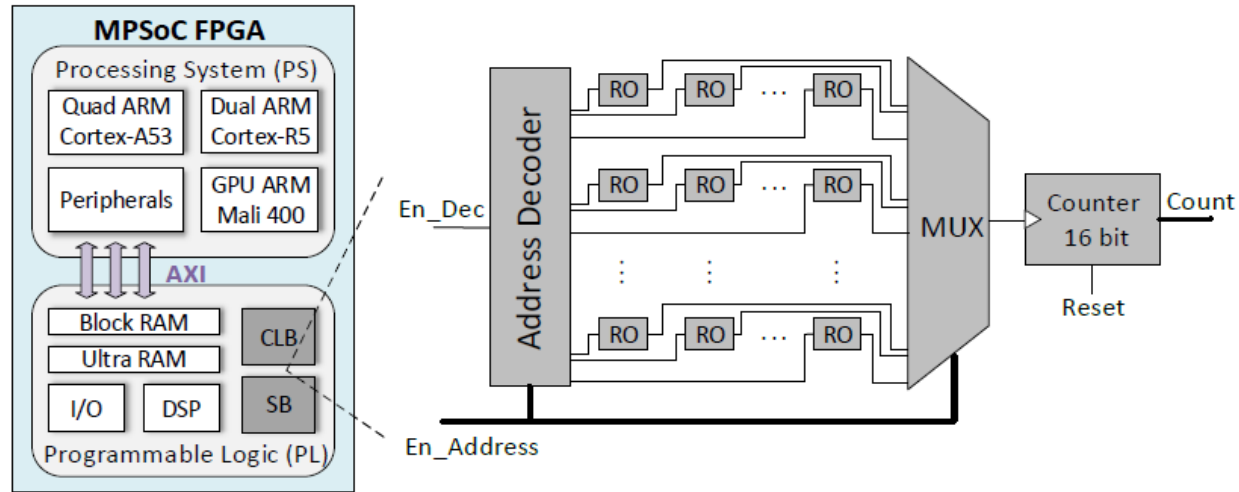
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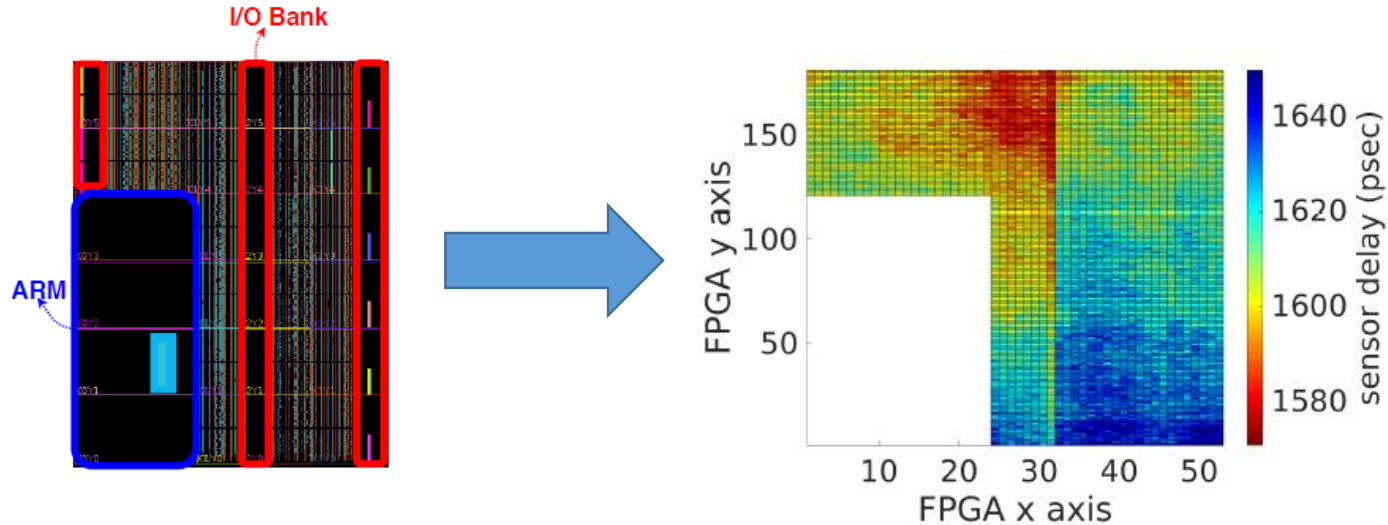
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 - Exploitation of variability offers significant opportunities for improved efficiency
- We evaluate the performance variation in 16nm FPGAs

Evaluation Methodology: Variability Maps



- Deploy a network of **soft macro sensors**

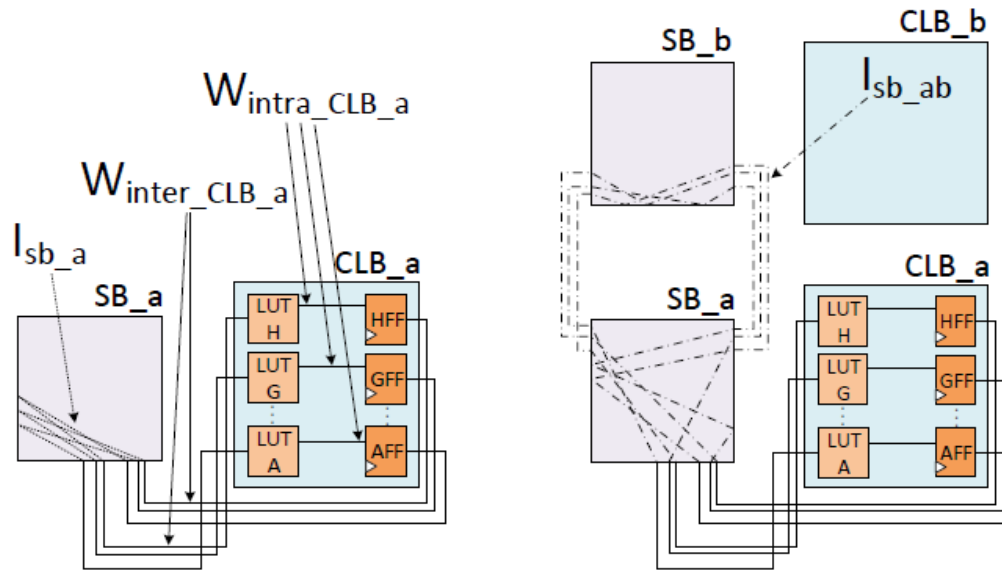
Evaluation Methodology: Variability Maps



- Deploy a network of **soft macro sensors**
- Compare the delay among the sensors:
 - inside the chip → **intra-die variation**
 - among the chips → **inter-die variation**

Evaluation Methodology: Sensor Design

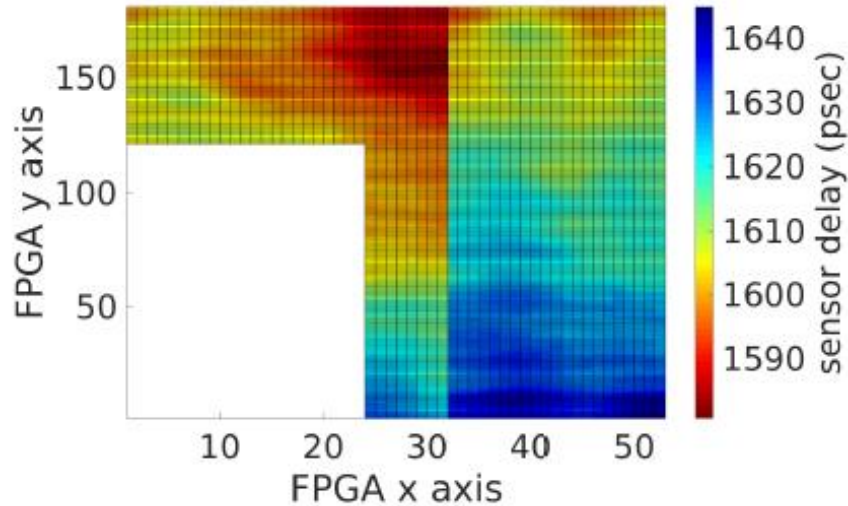
- Variety of **ring oscillator (RO)** sensors
 - Different utilization ratios of **logic & interconnect** resources



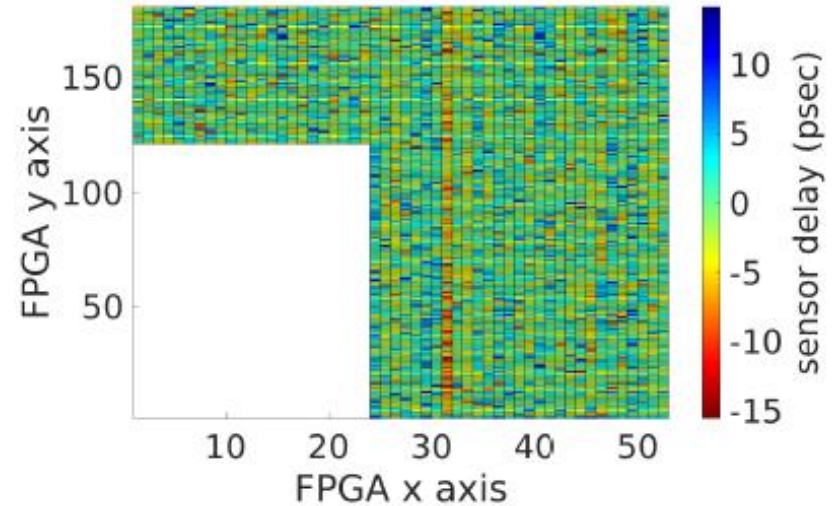
Evaluation Methodology: Decouple of Variability

- $T_d = T_d^S + T_d^R$

Systematic



Stochastic



Results: Total Variability Evaluation

- Four identical Zynq XCZU7EV FPGAs
 - 7.3% intra-die variation
 - 8.3% inter-die variation



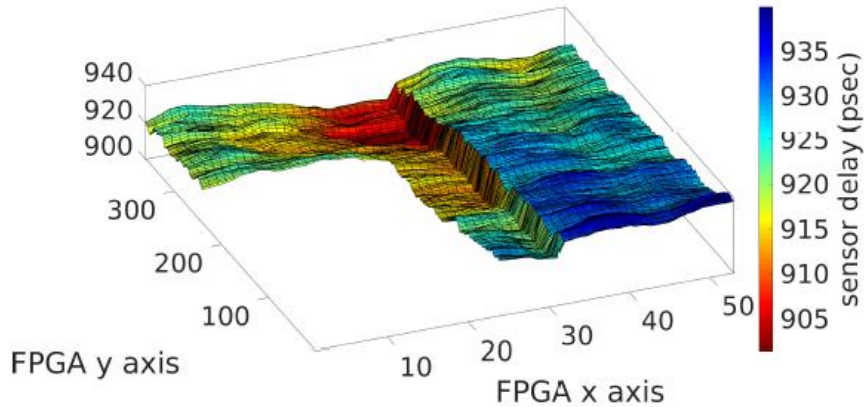
Results: Total Variability Evaluation

- Four identical Zynq XCZU7EV FPGAs
 - 7.3% intra-die variation
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- **Interconnects** present **lower variation**
 - e.g., 3.5% for intra-die
- **More pessimistic guard-bands** for interconnects

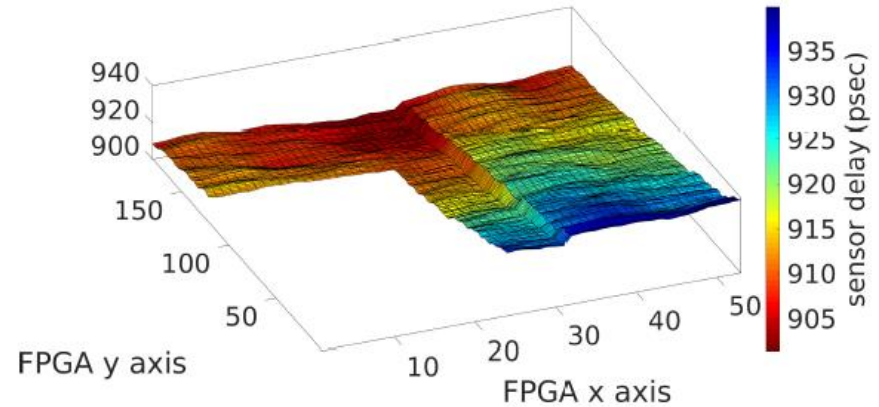


Results: Systematic Variability

Logic (mainly logic gates)



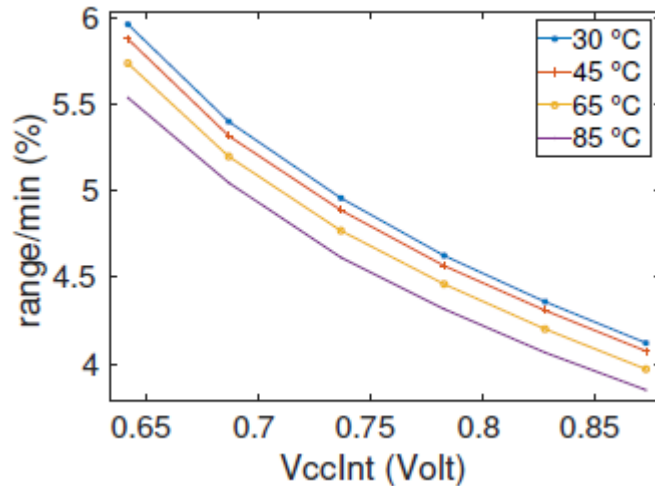
Interconnect (mainly wires)



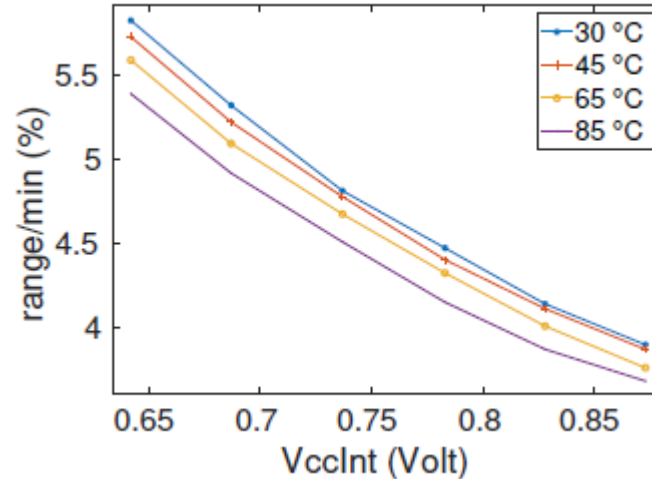
- **Correlation weakens** as logic/interconnect ratio changes, e.g., $p = 0.6$
- **High perf. estimation error** between different areas, e.g., 3.45%

Results: Variability Under Diverse Conditions

Logic (mainly logic gates)



Interconnect (mainly wires)



- Increase with voltage reduction, decrease with temperature elevation
- Increased performance estimation error, i.e., 3.6%

Conclusion

1. Study of performance **variation in 16nm FPGAs** in a multifaceted way
 - various sensors, operating conditions and decoupling of variability
 - up to **10% intra-die** and **12% inter-die** variation

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 - various sensors, operating conditions and decoupling of variability
 - up to **10% intra-die** and **12% inter-die** variation
2. **Unequal variability** results for **logic & interconnect** resources
 - weak correlation, high performance estimation error
 - logic resources present higher variation (systematic & stochastic)
3. Insights for the implementation of **more accurate mitigation methods/tools**

Thank you!

