Preallocating Resources for Distributed Memory based FPGA Debug

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FPGA Debug - Logic Analyzer

1. External?
2. Internal?
   - Time
   - Resources
Xilinx Internal Logic Analyzer (ILA)
FPGA with 94% of LUT resources utilized:

Xilinx ILA:

Where will the embedded logic analyzer fit?
Can we debug at all?
Xilinx Shift Register LUT (SRL)
Distributed Memory (DIME) Debug

SRL0

USER LOGIC

SRL1
4-bit Counter Output
DIME Debug - Research Questions

1. Can we enable internal debug when the device is 90%+ utilized?

2. How will DIME trace buffers impact the user circuit (timing)?

3. What is the ideal organization of DIME buffers on the device?
How do we organize those LUTs?
DIME Preallocation - Research Questions

1. Will this hurt the performance of the user circuit?

2. Will this improve performance of the combined DIME + user circuit?
Benchmarks

LC3
Sudoku
RPulseG
RNG
uFIFO
Preallocation - Affect User Design?

- Implementation: No impact
- Timing: Max 0.1ns

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Original min. period</th>
<th>Prealloc min. period</th>
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</thead>
<tbody>
<tr>
<td>LC3 70%</td>
<td>4.9ns</td>
<td>5.0ns</td>
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<tr>
<td>LC3 80%</td>
<td>5.2ns</td>
<td>5.2ns</td>
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<tr>
<td>LC3 90%</td>
<td>6.2ns</td>
<td>6.3ns</td>
</tr>
<tr>
<td>Sudoku 75%</td>
<td>6.6ns</td>
<td>6.7ns</td>
</tr>
<tr>
<td>Sudoku 94%</td>
<td>7.0ns</td>
<td>6.9ns</td>
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<tr>
<td>RNG 70%</td>
<td>1.6ns</td>
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<td>1.6ns</td>
<td>1.7ns</td>
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<tr>
<td>uFIFO 70%</td>
<td>3.5ns</td>
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<td>uFIFO 80%</td>
<td>3.8ns</td>
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Preallocation - Affect DIME Debug?

LC3 90%

LC3 90% (with preallocation)
Results

RPulseG

Sudoku

uFIFO

RNG
Can we lengthen DIME trace buffers?

RPulseG

Sudoku

uFIFO

RNG

LC3
Conclusion

- DIME debug: 90%+ utilized designs
- Preallocating FPGA resources for DIME debug:
  - Almost no impact on original design
  - Reduce timing penalty (up to 2ns)
  - Increase trace buffer count (up to ~3x)
- DIME trace buffers can be lengthened
Thank you

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Contributions

- Pros/cons of preallocating LUTs for DIME trace buffers
- 5 unique (duplication-based) benchmarks
- Extending DIME trace buffers to 256 bits
Experiments

<describe experiments>

<diagram?>
DIME Debug - Research Questions

1. How many user signals can I access?

2. How big are the trace buffers?

3. What is the impact to the user circuit (timing)?
Pinterest FPGA:
Can we lengthen DIME trace buffers?
Real FPGA:

Where will the embedded logic analyzer fit?
Experiments

Will preallocating resources improve the distributed-memory debug process?

- Timing?
- Debug bits?