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Post-layout evaluation us architecture Flow runs in 24h	ing a comm	ercial 40	nm node :	and a Stra	itix IV-lik
Using an optimized cell li	brary (multip	lexers, 0	CCFF):		
 3x delay reduction 	Path Type Delay (ns)	Previous work [1]	OpenFPGA (TT)	OpenFPGA (SS)	Stratix IV
	5-LUT	0.46 (+70%)	0.14 (-48%)	0.26 (-3%)	0.27 (100%)
	6-LUT	0.5 (+78%)	0.15 (-46%)	0.27 (-3%)	0.28 (100%)
	1-bit Adder	0.7 (-9%)	0.54 (-30%)	1.00 (+30%)	0.77 (100%)
	20-bit Adder	1.63 (+32%)	1.10 (-6%)	2.12 (+72%)	1.23 (100%)
	Local Routing	0.27 (+58%)	0.12 (-30%)	0.23 (+35%)	0.17 (100%)
20x20 FPGA	L-4 track	2.53 (+328%)	0.40 (-32%)	0.75 (+27%)	0.59 (100%)
200201104	L-16 track	4.02	0.78	1.55	1.02





OpenFPGA: Summary

Fully functional XML to Prototype flow (FPGA-X2P) supporting homogenous multi-mode FPGA fabrics

XML-to-Verilog generator

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- Verilog-to-Bitstream generator
 Verilog testbenches for functionality/formal validation
- veniog testoenenes for fanotionality/formal validatio
- Automatic backend flow for homogenous FPGA
- 20 × 20 FPGA layout using a commercial 40nm node in 24h
- 2 × area and 3 × performance improvement over previous arts

OpenFPGA alpha release with tutorials

Github repository: https://github.com/LNIS-Projects/OpenFPGA
 Online documentation: https://openfpga.readthedocs.io/en/mast



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Pierre-Emmanuel Gaillardon and Xifan Tang have financial interests in the company ReRouting LLC, which manufactures RRAM-based systems and provides engineering service.

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