Quantifying the Benefits of Dynamic Partial Reconfiguration for Embedded Vision Applications

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FPGAs mostly used as substitutes for ASICs.

Less power/energy efficient than ASIC

Runtime reprogrammable 😊

Use REprogrammability to be more than substitute for ASICs
Realtime and Interactive Applications

- Many different tasks not needed at the same time.
- Efficiency (area, cost, power and energy) as important as meeting performance requirements.

Mapping tasks statically on a large FPGA is inefficient.
A dynamic solution on a small FPGA is more efficient than a static solution on a large FPGA.
Quantify DPR Benefits on Smaller FPGA vs Static Mapping on Larger FPGA

- Two apps. w/ real-time requirements (60 fps@1080p).

  **Interactive app**
  - 4 sets of tasks (15 tasks total)
  - **Infrequent** reconfigurations (minute to hour reconfig. interval)

  **Navigation app**
  - 6 sets of tasks (6 tasks total)
  - **Frequent** reconfigurations (millisecond reconfig. interval)

⇒ How much savings in area, device cost, power, energy?
⇒ How much when ratio of reconfig. to compute 1:1?
Area, Cost and Power/Energy Savings

- Interactive application
  - ~3x logic saving (10x $ saving in parts cost)
  - ~30% power/energy saving

- Navigation application
  - ~3.5x logic saving (7x $ saving in parts cost)
  - ~30% power/energy saving even when ratio of reconfig. to compute 1:1
For more information, come to the poster session.

Thanks!